Xyce™ Parallel Electronic Simulator Release Notes

Release 3.0

Sandia National Laboratories

Xyce™ Parallel Electronic Simulator Release Notes

Release 3.0

Eric R. Keiter, Scott A. Hutchinson, Robert J. Hoekstra, Richard L. Schiek, and Eric Rankin
Electrical and Microsystems Modeling

Thomas V. Russo, Carolyn W. Bogdan, and Steven D. Wix
Component Information and Models

David N. Shirley and Phillip M. Campbell
Scientific Computing Systems

Sandia National Laboratories
P.O. Box 5800
Mail Stop 0316
Albuquerque, NM 87185-0316

Scope/Product Definition

The **Xyce** Parallel Electronic Simulator has been written to support, in a rigorous manner, the simulation needs of the Sandia National Laboratories electrical designers. Specific requirements include, among others, the ability to solve extremely large circuit problems by supporting large-scale parallel computing platforms, improved numerical performance and object-oriented code design and implementation.

The **Xyce** release notes describe:

- Hardware and software requirements

- New features and enhancements

- Any defects fixed since the last release

■ Current known defects and defect workarounds

For up-to-date information not available at the time these notes were produced, please visit the **Xyce** web page at http://www.cs.sandia.gov/xyce.

Hardware/Software

This section gives basic information on supported platforms and hardware and software requirements for running **Xyce** 3.0.

Supported Platforms

Xyce 3.0 currently supports any of the following operating system (all versions imply the earliest supported – **Xyce** generally works on later versions as well) platforms. These platforms are supported in the sense that they have been subject to certification testing for the **Xyce** version 3.0 release.

■ SGI IRIX® 6.5.3, Workshop Compilers 7.4.2 (serial and parallel using SGI MPI)

■ Redhat Linux®, Enterprise version 9.0 on Intel Pentium® architectures (serial and parallel using MPICH version 1.2.5.2 or LAM MPI version 7.0.6)

■ Tru64 on HP/Compaq Alpha® (serial and parallel)

■ FreeBSD on Intel Pentium® architectures (serial and parallel using MPICH or LAM MPI)

■ Microsoft Windows® (serial)

■ Apple® OS X (serial)

Build Capability but Not Supported

The platforms listed in this section are "not supported" in the sense that they are not subject to nightly regression testing, and they also were not subject to certification testing for the **Xyce** version 3.0 release. For large parallel platforms, such as ASCI White, this sort of testing is not a realistic option. These platforms are supported in the sense that **Xyce** 3.0 has been built for these platforms, and successfully executed on them. If a user needs to run **Xyce** 3.0 on one of these platforms, contact the **Xyce** team and we will work with you on a case-by-case basis.

■ ASCI White (IBM) (parallel)

■ Sandia Institutional Computational Clusters (serial and parallel).

Hardware Requirements

The following are estimated hardware requirements for running **Xyce**:

- 128MB memory recommended, 64 MB memory minimum – *memory requirements increase with circuit size*

- 50MB disk space (not including space needed for output files)

Software Requirements

Several libraries (all freely available from Sandia National Laboratories and other sites) are required to build **Xyce** on a platform. These are only required when building **Xyce** from source. These are:

- Trilinos Solver Library (Sandia, http://software.sandia.gov/Trilinos) . This is a suite of libraries including Amesos, KLU, AztecOO, Belos, Epetra, EpetraExt, Ifpack, NOX, LOCA, and y12m.

- SuperLU (http://www.nersc.org)

- Xyce Expression library (libexpr.a).

- BLAS (libblas.a).

- LAPack (liblapack.a).

For parallel builds, the following are additionally required:

- MPI (http://www-unix.mcs.anl.gov/mpi/) library for message passing (version 1.1 or higher), such as MPICH or LAM. The version used to build Xyce must be the same that is used for building Trilinos.

- Zoltan (Sandia, http://www.cs.sandia.gov/Zoltan) and its associated libraries (libzoltan.a, libzoltanCPP.a, libparmetis.a, libmetis.a)

Xyce Release 3.0 Documentation

The following **Xyce** documentation is available at the **Xyce** internal website in pdf form. Some of this documentation is in "Draft" mode and is incomplete.

- **Xyce** Users' Guide, Version 3.0

- **Xyce** Reference Guide, Version 3.0

■ **Xyce** Release Notes, Version 3.0

■ **Xyce** Theory Document

■ **Xyce** Test Plan

New Features and Enhancements

This release is the first release following the Version 2.1 release. It encompasses many key bug fixes as well as key robustness and performance enhancements. Highlights for this release include:

■ Stability enhancements to the prompt photocurrent models and additional photocurrent models.

■ Enhanced MOSFET-based homotopy algorithms for DCOP solution.

■ New device models: BSIMSOI, pn-junction photocurrent source, JFET Level 2, MESFET, generic switch.

■ More advanced temperature compensation for JFET, MESFET, capacitor, inductor.

■ Improved numerical stability in the level-1 JFET, and VDMOS devices.

■ Improved parser scalability, and error reporting.

■ Updated Trilinos solver library.

■ New, variable-order, variable stepsize time integrator (optional).

■ Support for linking Xyce to IC-CAP.

■ Support for random numbers in expressions via the RAND() function.

For details of each of these new features, see the **Xyce** Users' Guide, and the **Xyce** Reference Guide.

Device Support

Table 1 contains a complete list of devices for **Xyce** Release 3.0. A number of the devices have been revised to improve robustness, and additional model levels for some devices have been added (the level=2 JFET and the level=10 MOSFET). Two new device types, the MESFET and the generic switch have also been added for **Xyce** Release 3.0.

Device	Comments
Capacitor	Age-aware, semiconductor

Device	Comments
Inductor	Nonlinear mutual inductor (see below)
Nonlinear Mutual Inductor	Sandia Core model (not fully PSpice compatible) **New!** Stability improvements.
Resistor	Semiconductor
Diode (Level 1)	
Diode (Level 3)	Prompt photocurrent radiation model
Diode (Level 4)	**New!** Generic photocurrent source model
Independent Voltage Source (VSRC)	
Independent Current Source (ISRC)	
Voltage Controlled Voltage Source (VCVS)	
Voltage Controlled Current Source (VCCS)	
Current Controlled Voltage Source (CCVS)	
Voltage Controlled Current Source (CCCS)	
Nonlinear Dependent Source (B Source)	
Bipolar Junction Transistor (BJT) (Level 1)	
Bipolar Junction Transistor (BJT) (Level 2)	Prompt photocurrent radiation model.
Bipolar Junction Transistor (BJT) (Level 3)	Neutron-effects model.
Bipolar Junction Transistor (BJT) (Level 4)	Prompt photocurrent radiation model (same as level 2).
Junction Field Effect Transistor (JFET) (Level 1)	SPICE-compatible JFET model.
Junction Field Effect Transistor (JFET) (Level 2)	**New!** Shockley JFET model.
MESFET	**New!**
MOSFET (Level 1)	
MOSFET (Level 3)	
MOSFET (Level 9)	BSIM3 model. **New!** Initial condition support.
MOSFET (Level 10)	**New!** BSIM SOI model with initial condition support.
MOSFET (Level 18)	VDMOS model.
MOSFET (Level 19)	VDMOS photocurrent model.

Device	Comments
Transmission Line	Lossless.
Controlled Switch (S,W) (VSWITCH/ISWITCH)	**New!** Voltage or current controlled.
Generic Switch (SW)	**New!** Controlled by an expression.
PDE Devices (Level 1)	one-dimensional
PDE Devices (Level 2)	two-dimensional

Table 1: Devices Supported by Xyce.

Robustness Improvements

■ Improvement of homotopy algorithms has for large MOSFET circuits, including SOI circuits.

■ The radiation models (Level 3 Diode and Level 2 BJT) have been made less susceptible to roundoff error, and now support breakpoints for discontinuity capturing.

New Device Types

■ The SPICE-compatible MESFET model.

■ A generic switch device, which can be controlled by current, voltage or an expression.

New Model Levels

■ The level 4 photocurrent BJT introduced in Release 2.1 has replaced the Level 2 of previous releases — in Release 3.0 the level 2 BJT is the same as the level 4.

■ Level 10 MOSFET, Berkeley BSIM SOI (Silicon on Insulator) model version 3.2.

■ Level 9 and 10 MOSFET's support initial conditions on junction voltages.

■ The level 4 diode is a generic pn-junction photocurrent source. It can be used to introduce basic photocurrent effects in any device that has a PN junction. It contains only the photocurrent source terms from the level 3 diode.

■ Level 2 JFET, based on Shockley's original formulation that is more accurate than the SPICE-compatible Level 1 JFET.

Improved Temperature Compensation

■ The JFET and MESFET employ quadratic temperature coefficients for the DC model parameters. The temperature coefficients must be obtained from data by parameter extraction in the same way the other model parameters are obtained.

■ The capacitor and inductor now have quadratic temperature coefficients.

Enhanced Solver Stability and Features

■ Xyce now uses an enhanced version of the Trilinos solver library version 4.0.

■ The KLU direct linear solver, which was specifically designed for circuits, is now the default in Xyce. KSPARSE, the previous default solver, remains available and can be selected with a command line option or netlist command.

■ A new variable-order (maximum order=5), variable timestep time integrator is available in **Xyce**. This time integrator is not the default, but can be enabled from the command line. This new time integrator can potentially run much faster than the default time integrator, particularly on oscillatory circuits.

Interface Improvements

■ The netlist parser has been further optimized for large parallel runs.

■ Current through two lead devices and lead currents in three or more lead devices can be output in .PRINT line.

■ Support for *.raw output files.

■ Support for linking Xyce to IC-CAP.

Defects of Release 2.1 Fixed in this Release

Defect	Description
Breakpoints are not generated for dependent sources. [Bug 265]	Breakpoints are now generated from time dependent expression in dependent sources. This corrects many problems where critical circuit behavior from events was previously missed.
Parsing errors can lead to parallel hangs. [Bug 765]	Error handling has been greatly improved for parallel runs.
Node/device name collisions cause catastrophic erors. [Bug 767]	Name collisions and duplicate names are now detected early, and exit cleanly with informative fatal errors.
Incomprehensible errors when nodes are used in .param expressions. [Bug 769]	Error handling for this illegal usage is now informative.
Incorrect substitution of nodes in .subckt. [Bug 785]	Errors that occurred when the names of substituted and other nodes were coincidentally the same on the .subckt line are corrected.
Mulitply-coupled Mutual Inductances not coupled correctly. [Bug 677]	Errors could occur when multiple inductors (more than two) were coupled together. This was a parsing error which has been fixed.
DOS-Style line breaks cause mis-parsing of input [Bug 689]	The windows build of Xyce 2.1 had trouble with DOS-style line breaks. This has been fixed for Xyce 3.0.
Add temperature effects to capacitor and inductor. [Bug 644]	Quadratic temperature compensation added to these devices.
Initial JFET voltage drops imposed incorrectly. [Bug 674]	This problem has been corrected.
JFET Capacitor currents not handled correctly. [Bug 669]	This bug has been fixed and verified.
Limiter functions used by the JFET are inconsistent with SPICE. [Bug 670]	The bug is fixed and marked verified.
Use of gmin in the JFET not consistent. [Bug 675]	This problem has been fixed.
Fix MESFET with respect to capgs and also gm. [Bug 684]	Bug is fixed and verified.

Table 2: Fixed Defects.

Known Defects and Workarounds

Defect	Description
.DC sweep output.	.DC sweep calculation does not automatically output sweep results. *Workaround:* Use .PRINT statement to output sweep variable results.
Failure for netlists using ChileSPICE digital primitives.	**Xyce** does not currently support the use of digital primitives.
BJT Current Crowding	"Timestep too small" failures can result when IRB nonzero with level 2 and level 4 BJT *Workaround:* If such failure observed, disable current crowding effect by setting IRB to zero in all BJT models. Please feed back such circuits to the **Xyce** development team so that this bug can be characterized and eliminated.
Microsoft Windows installation restrictions	Users with insufficient privileges (i.e. Limited Account) are not permitted to install **Xyce** into folders on the System Drive (usually C:). *Workaround:* First, manually create the desired folder on the System Drive. It is then possible to install **Xyce** into this folder by following the standard Setup procedure.
MPICH parallel runs may not exit cleanly	**Xyce** may not exit cleanly if it encounters certain errors during parsing. *Workaround:* If **Xyce** appears to hang, manually terminate each process. Usually a SIGTERM or ^C is sufficient to halt the job. Users running on the Alpha should manually check for zombie processes after **Xyce** error exits, and kill them if necessary.
Incompatible proprietary file formats.	Netlists created with programs like Microsoft Word and Microsoft Wordpad will not run in **Xyce**. **Xyce** does not recognize proprietary file formats. *Workaround:* It is best not to use such programs to create netlists, unless netlists are saved as *.txt files. If you must use a Microsoft editor, it is better to use Microsoft Notepad. In general, the best solution is to use a Unix-style editor, such as Vi, Gvim, or Emacs.
Expressions in the .PRINT line can't use variables specified by .PARAM statements.	Specifying expressions in the .PRINT line is a new **Xyce** capability. It is very useful, but is unable to use .PARAM variables. *Workaround:* For now, the only solution is to not use .PARAM variables in .PRINT statement expressions. This will be fixed for a later release.

Defect	Description
One known instance of restart results not matching original run results.	There is one case for a customer's parallel run of a large digital circuit of BSIM3's where the restart output does not match the original results for the same time range. *Workaround:* The only choice for now is to check the restart results against the baseline results for some block if the run results have a very tight tolerance for success. It is suggested to overlap the original run time with the restart time allowing comparison.
Duplicate node names in `.SUBCKT` [bug 784]	Duplicate node names in a `.SUBCKT` specification will lead to incorrect results. Users must take care that all nodes specified on a `.SUBCKT` line are unique in Xyce 3.0.
Lead currents in B/E/F/G/H source and switch expressions [bug 801]	Use of lead currents in B/E/F/G/H source and switch expressions will lead to incorrect results. A fatal diagnostic should be generated for such usage, but is not. The only supported use of lead currents is on `.PRINT` lines in Xyce 3.0.
Use of multiple YPDE, YDAC, and YADC devices improperly flagged as duplicate device error [Bug 803]	The test for duplicate devices improperly reports that two Y devices of the same type are duplicates of each other without checking the second field (where the actual device name is). This will be fixed in the minor update release (Xyce 3.0.1). In the meantime, the only workaround is to place the devices in separate subcircuits, in which case they will be prefixed with the subcircuit name and not mistakenly identified as duplicates.

Table 3: Known Defects and Workarounds.

Incompatibilities With Other Circuit Simulators

Issue	Comment
`.SAVE` does not work.	**Xyce** does not support this. Use `.PRINT` instead.
`.OP` is not complete	A `.OP` netlist will run in **Xyce**, but will not produce the extra output normally associated with the `.OP` statement.
Pulsed source rise time of zero.	A requested pulsed source rise/fall time of zero really is zero in Xyce. In other simulators, requesting a zero rise/fall time causes them to use the printing interval found on the `.TRAN` line.
Mutual Inductor Model.	Not the same as PSpice. This is a Sandia developed model but is compatible with Cadence PSpice parameter set.
`.PRINT` line shorthand.	Output variables have to be specified as V(node) or I(source). Specifying the node alone will not work. Also, specifying V(*) or I(*) (to get all voltages or currents) will not work.
BSIM3 level.	In **Xyce** the BSIM3 level=9. Other simulators have different levels for the BSIM3.
BSIM SOI v3.2 level.	In **Xyce** the BSIM SOI (v3.2) level=10. Other simulators have different levels for the BSIM SOI.
Node names vs. device names.	Currently, circuit nodes and devices MUST have different names in **Xyce**. Some simulators can handle a device and a node with the same name, but **Xyce** cannot.
Interactive mode.	**Xyce** does not have an interactive mode.
ChileSPICE-specific "operating point voltage sources."	These are not currently supported within **Xyce**. *However...* **Xyce** does support "`IC=<value>`" statements for capacitors, inductors, and the two BSIM devices which will automatically set these voltage drops at the beginning of a transient simulation.
Syntax for `.STEP` is different.	The manner of specifying a model parameter to be swept is slightly different. Also, it is not possible to do a .STEP sweep over a global parameter. See the Users' and Reference Guides for details.

Table 4: Incompatibilities with other circuit simulators.

Important Changes to **Xyce** Usage Since the Last Release.

Table 5 lists some usage changes for **Xyce**.

Issue	Comment
The TCAD/PDE devices no longer use the letter "Z" as their identifier in the nelist.	This has been changed to "YPDE". This was done to allow for the MESFET to use the letter "Z", to maintain compatibility with SPICE. [Bug 655]

Table 5: Changes to netlist specification since the last release.

Acknowledgements

The authors would like to acknowledge the entire Sandia National Laboratories HPEMS (High Performance Electrical Modeling and Simulation) team, including Steve Wix, Carolyn Bogdan, Regina Schells, Ken Marx, Steve Brandon and Bill Ballard, for their support on this project. We also appreciate very much the work of Jim Emery, Becky Arnold and Mike Williamson for the help in reviewing this document.

Lastly, a very special thanks to Hue Lai for typesetting this document with LATEX.

Trademarks

Contacts

Bug Reports	http://tvrusso.sandia.gov/bugzilla
Email	xyce-support@sandia.gov
World Wide Web	http://www.cs.sandia.gov/xyce